WHAT IS CLAIMED IS:

1. A data processing system for executing a program having branch instructions therein, each branch instruction specifying a target address in said program defining an instruction that is to be executed if that branch instruction causes said program to branch, said data processing system comprising:

a plurality of processing sections, each processing section comprising:

a local memory for storing instruction sequences from said program that are to be executed by that processing section, said instruction sequences comprising instructions of different lengths;

a function unit for executing instructions stored in said local memory; and

a pointer containing a value defining the next instruction in said local memory to be executed by said function unit, wherein

each processing section executes part of said program;

each function unit executes instructions synchronously with said other function units; and

said pointers in each of said processing sections are reset to a new value determined by said target address of one of said branch instructions when a function unit branches in response to that branch instruction.

2. The data processing system of Claim 1 further comprising a memory for storing a mapping for each target address in said program specifying one of said pointer values for each of said pointers corresponding to that target address.

3. The data processing system of Claim 1 wherein said program is divided into super instructions, each super instruction comprising a linear block of code that can only be entered

at a starting address corresponding to said block of code and each block of code having one or more branch instructions, at least one of said branch instructions having a target address corresponding to a super instruction in said program.

4. The data processing system of Claim 1 wherein one of said super instructions comprises one instruction for each processing section to be executed on each clock cycle.

5. The data processing system of Claim 1 wherein said local memory of one of said processing sections comprises a cache memory.